Total Harmonic Distortion Reduction of 9-Level Packed E-Cell (PEC9) Inverter

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Abstract- In this paper phase-shift PWM technique (PS-PWM) is applied to reduce total harmonic distortion (THD) of PEC-9 inverter and the results have been compared with the level-shift PWM method (LS-PWM). PEC-9 inverter consists of one voltage source, seven active devices and one DC-link which contains two capacitors where each of them must be balanced to one-quarter of Dc source to achieve nine output level. Active balancing method for capacitors was integrated with PS-PWM and the regulation was carried out through redundant switching states of PEC-9. Each output level of the inverter is produced via comparing a set of carrier waveforms with one reference signal. The PS-PWM and LS-PWM techniques have been applied for PEC-9 using MATLAB/SIMULINK program. With 5mH L-filter, the THD of LS-PWM was determined as 2.28%, while THD for PS-PWM was 0.34%.

Keywords- Phase shift-PWM, PEC9, level shift-PWM, single DC-source multilevel Inverter, harmonic reduction

1. Introduction

These days, multilevel inverters (MLIS) are becoming more utilized and more investigated because of their amazing characteristics. They produce step-wave output voltage using DC sources and active power devices and they have been applied for wide range of high, low, and medium power applications. Increasing the number of output levels makes the form of output signal smoother and closer to sinusoidal shape, therefore decreasing the THD of output signal and minimize the size of the output filters. Moreover, MLIS not only enhance the output quality but also reduce voltage stress on active devices. In spite of the fact that, there are some drawbacks for multilevel inverters, such as more elements that increase the overall complexity and cost of the system. However, with recent progressions in this field, these drawbacks can be handled [1-3].

From the three most common traditional topologies NPC, FC, and CHB, many inverters have been introduced. A lot of studies concentrated on obtaining more output levels with minimum circuit complexity by proposing new topologies [4]. In [5-6] for asymmetrical multilevel inverters, an envelope E-type and a square T-type have been proposed. With two sources, K-type has also been presented in [7]. However, they have large number of voltage sources, so they are limited for some applications. In [8-10] several creative MLIs have been reported to generate various levels, but they suffer from a large number of elements. The single voltage source and compact topology for MLIs have been extensively studied as a practical and economical compared to other inverters [11-13].

Packed U-Cell (PUC) inverter was proposed in [14], it can produce seven output-levels by regulating the DC-Link voltage to one-third of Dc source, or five output-levels generated by self-capacitor balancing to half of the DC input source [15-16]. In [17] the PEC-9 inverter was proposed to achieve nine output-levels with one DC source and one DC-Link which actively regulated to half of input Dc source. Thus, each capacitor in the DC-Link naturally regulated at one-quarter of the main source. Seven and five output-levels can also be obtained from PEC-9 inverter.

Various modulation strategies with a large frequency range have been reported for MLIs. Lately LS-PWM and PS-PWM techniques are most widely used in switching strategy. In these methods many carrier waves compared with a reference signal and produce desired switching gate signals. In PS-PWM, switching harmonics contents is shifted to higher orders, making it possible to improve harmonic performance compared to LS-PWM [18]. In this paper, the LS-PWM and PS-PWM are implemented for PEC-9 to achieve a minimum

THD for the output waveform. Section II demonstrate the PEC-9 switching states and its basic configuration. In section III, explains the switching strategy methods for PEC-9. The results of the simulation of the modulation methods used are shown in section IV.

2. Single Phase PEC-9 Topology and Active Voltage Balancing

The nine level PEC-9 inverter shown in Fig. 1. It consists of six active devices, a four-quadrant switch, single DC source and one DC-Link contains two capacitors placed in row, which both can be accordingly charging and discharging. Redundant switching states allow the voltage of the DC-Link to be balanced to one-half of the Dc source. Therefore, each capacitor balanced to one quarter of the source to generate nine output levels. Active balancing of the DC-Link illustrated in Fig. 2. Half of the DC source is compared with the

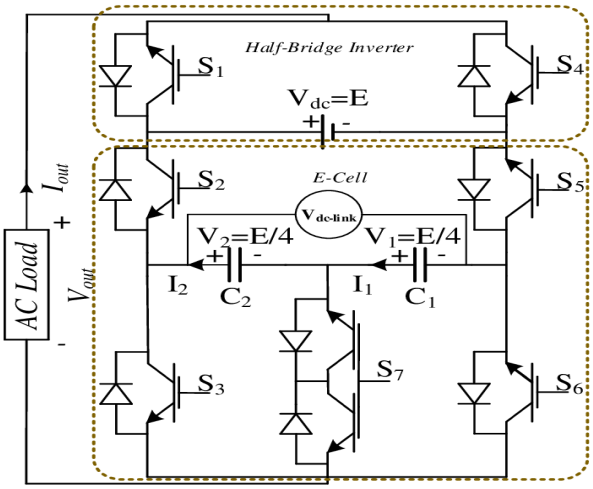


Fig. 1. PEC-9 topology [17]

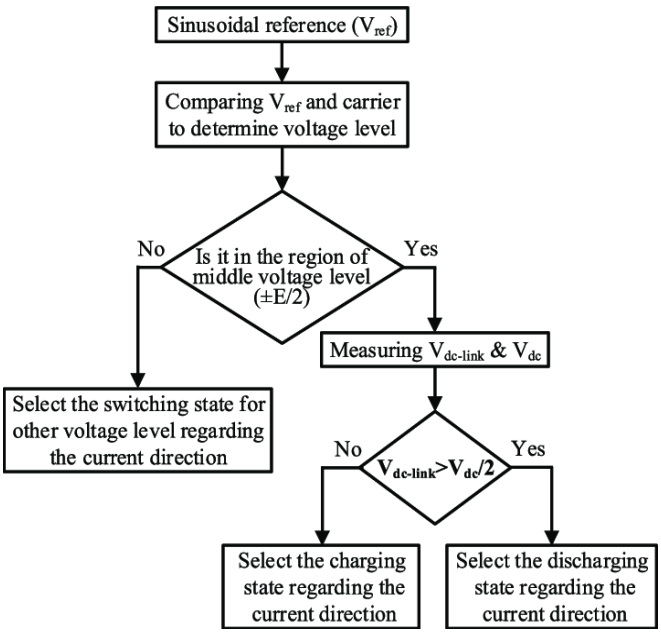


Fig. 2. Active balancing algorithm [20]

measured DC-Link voltage, and therefore selects the appropriate switching states. In this way, the balancing approach was integrated with the PWM technique to adjust the voltage of the capacitor. Table I lists the possible switching states, as well as the charging and discharging for each capacitor [17].

Table 1. The PEC9 switching states and voltage levels ('–' means neutral, '↑' means charging, and '↓' means discharging) [19]

No.	S_1	S_2	S_3	S_4	S_5	S_6	S_7	C_1	C_2	V_{out}
1	1	0	0	0	1	1	0	–	–	V_{dc} = +E
2	1	0	0	0	1	0	1	↑	–	$V_{dc} - V_1$ = +3E/4
3	1	0	1	0	1	0	0	↑	↑	$V_{dc} - V_1 - V_2$ = +E/2
4	1	1	0	0	0	1	0	↓	↓	$V_1 + V_2$ = +E/2
5	1	1	0	0	0	0	1	–	↓	V_2 = +E/4
6	0	0	0	1	1	1	0	–	–	0
7	1	1	1	0	0	0	0	–	–	0
8	0	0	0	1	1	0	1	↓	–	$-V_1$ = -E/4
9	0	0	1	1	1	0	0	↑	↑	$-V_{dc} + V_1 + V_2$ = -E/2
10	0	1	0	1	0	1	0	↓	↓	$-V_1 - V_2$ = -E/2
11	0	1	0	1	0	0	1	–	↑	$-V_{dc} + V_2$ = -3E/4
12	0	1	1	1	0	0	0	–	–	$-V_{dc}$ = -E

3. PWM Switching Strategy

3.1. Phase Shift-PWM (PS-PWM)

PS-PWM is one of most popular modulation techniques for MLIs. Compared to other modulation strategies, PS-PWM allows to increase the inverter's switching frequency and consequently reduce the size and cost of the output filters. Additionally, PS-PWM minimize the total harmonic distortion THD in output signal by moving harmonic components away from the fundamental frequency. For output level m, the PS-PWM need to use (m-1) carrier waves with equal amplitudes and the same frequency. The carrier signals placed close to each other and shifted horizontally by phase displacement given in Eq. (1)

$$\Delta\varphi = \frac{2\pi}{m-1} \tag{1}$$

To generate nine output levels, eight carriers having $\pi/4$ phase shift are used to modulate the reference wave as shown in Fig. 3. The modulation index for PS-PWM expressed in Eq. (2)

$$m = \frac{V_{ref}}{C_{ri}} \tag{2}$$

Where C_{ri} specified for carrier waveforms and V_{ref} referred to reference signal. There are four pair of carriers each pair shifted by π. If the reference signal is larger than all pairs, +E is generated by activating corresponding switching states. If V_{ref} is less than one carrier pair, and is more than three other pairs, then +3E/4 is produced. By following this process, the other positive output levels are obtained. Zero level is produced when reference wave more than one carrier and fewer than the other one in pair. Moreover, the negative levels are achieved when the inverted conditions of positive levels

are used. That means when V_{ref} is less than all pairs, -E is produced by activating its switching state [18,20].

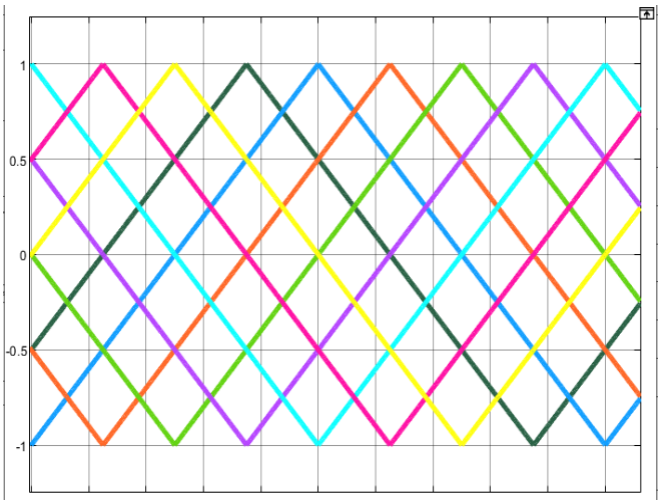


Fig. 3. Carrier signals for phase shift-PWM

3.2. Level Shift-PWM (LS-PWM)

There is many methods of multi-carrier SPWM, the simple one is phase disposition level shifted PWM (PDLS-PWM). For m output level inverter, m-1 triangular carrier signals with the similar amplitude A_c and frequency f_c should be ordered. In PDLS-PWM, sinusoidal reference signal has amplitude A_m and frequency f_m compared with each carrier signal, if the sinusoidal signal greater than one of carriers then the switches identical to that carrier are turned on, where each carrier related with appropriate output voltage level, and if the sinusoidal wave lower than one carrier then the switching devices according to that carrier are turned off. As shown in Fig. 4, this method has carrier signals shifted in level and they are in the same amplitude, frequency, and all of them are in phase [21].

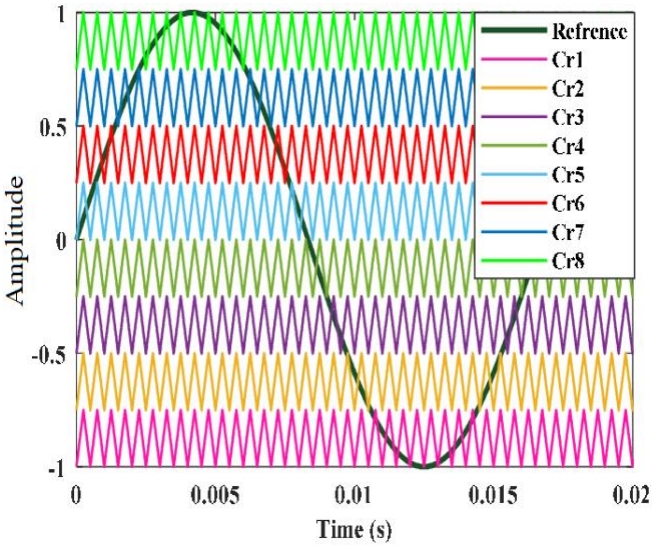


Fig. 4. Carrier signals for PDLS-PWM method [22]

The amplitude modulation index is defined as [23]

$$m_a = \frac{A_m}{(N-1)A_c} \quad (3)$$

Where A_m is the peak value of the reference wave, A_c is the peak magnitude of each carrier signal, and N is the number of converter levels.

4. Simulation and Results

MATLAB simulation program has been employed to simulate PEC-9 inverter to confirm the performance of the two modulation techniques PS-PWM and PDLS-PWM. The simulation parameters are provided in Table II. The results of applying PDLS-PWM method for PEC-9 involving load current, output voltage, and the DC-Link voltage have been represented in Fig.5 and Fig.6.

Table 2. Simulation parameters

DC Voltage Source	315V
Switching Frequency	25kHz
L-Filter	5mH
Capacitor	4700µF

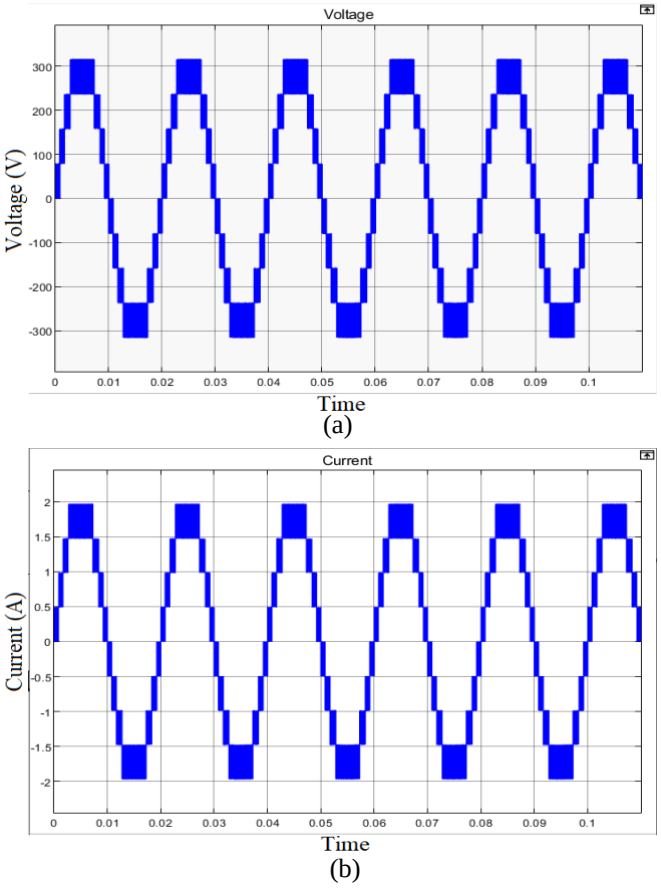


Fig. 5. Output waveforms for PDLS-PWM method; a) voltage; b) current

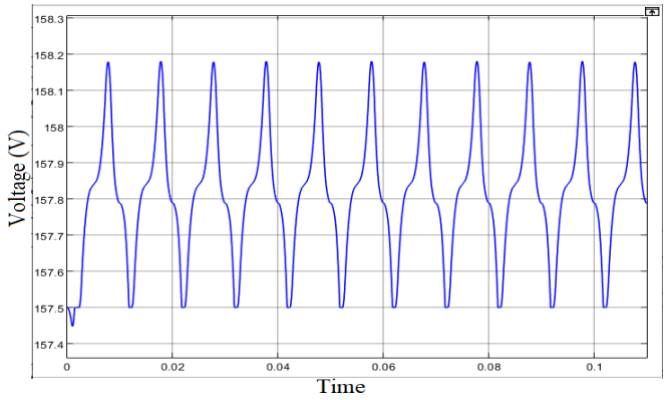


Fig. 6. The ripple of the DC-link voltage

As seen the voltage of the DC-Link has been regulated at half of the source. Fig. 7 display the FFT analysis for the output signal without filter. As indicated, the THD achieved by this method is equal to 14.22% and the first notable harmonics are begun from 25kHz where the switching frequency equal to 25kHz. After insert an inductor as a filter for PEC-9, the output signals and the FFT analysis are depicted in Fig.8 and Fig.9. It could be notice that the THD is reduced to 2.28%.

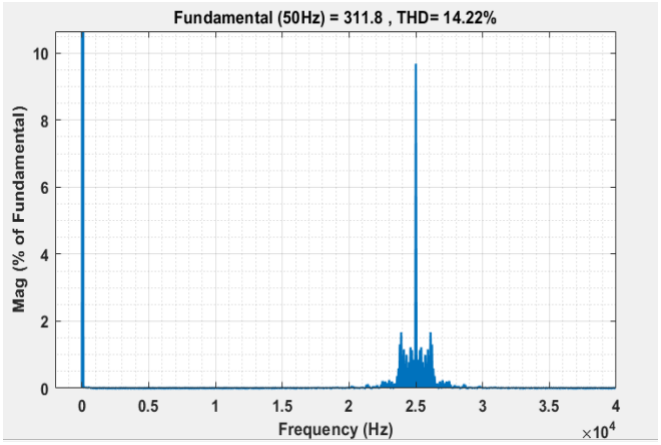
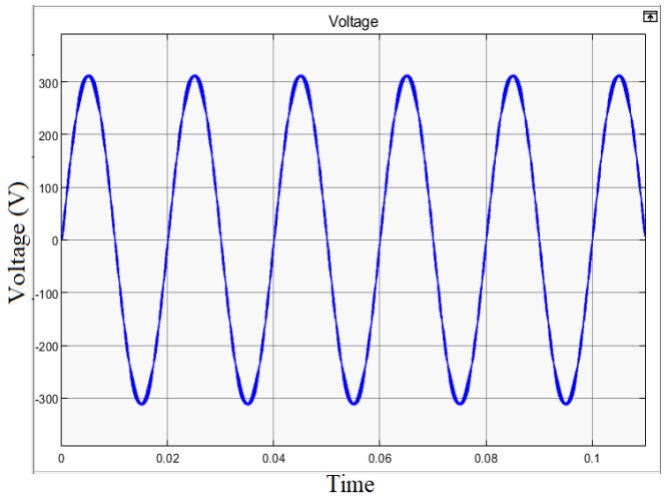
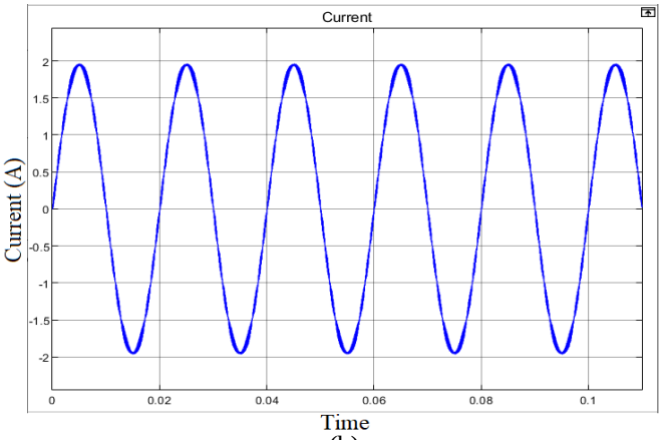


Fig. 7. FFT analysis of output signal for PDLS-PWM method



(a)



(b)

Fig.-8 Output signals for PDLS-PWM method with filter; a) voltage; b) current

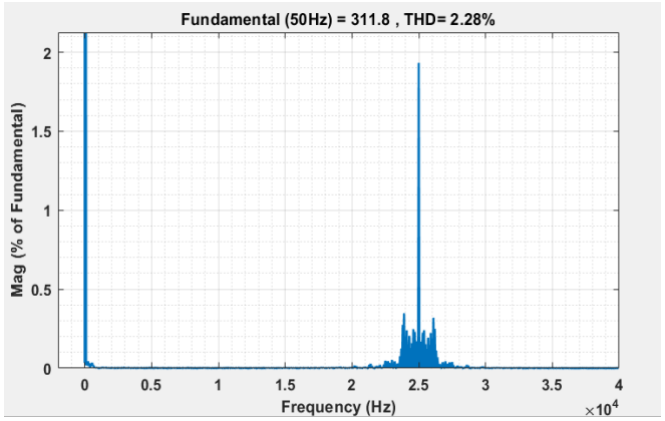
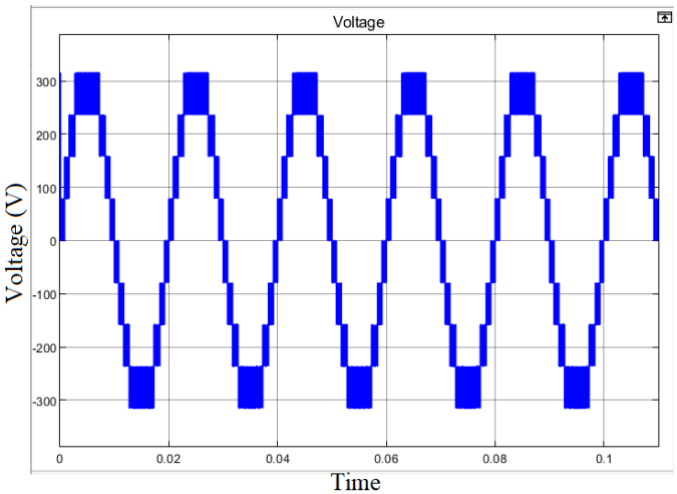
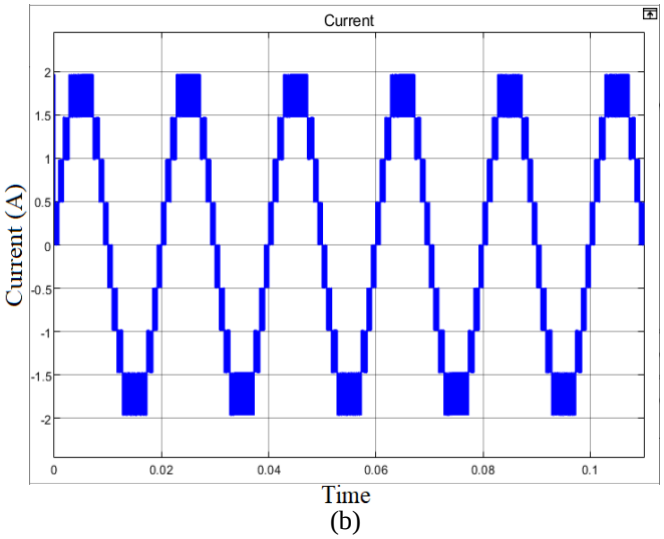


Fig. 9. FFT analysis for PDLS-PWM method with filter

The PS-PWM strategy has also been implemented for PEC-9 and the output results which contains output voltage, current signal as well as the voltage of the DC-Link displayed in Fig.10 and Fig.11. The spectrum analysis for the output waveform presented in Fig.12. As observed from the FFT analysis, the first obvious of harmonic contents has been located about 200kHz were shifted to 8-times of the carrier frequency.



(a)



(b)

Fig. 10. Output waveforms for PS-PWM method; a) voltage; b) current

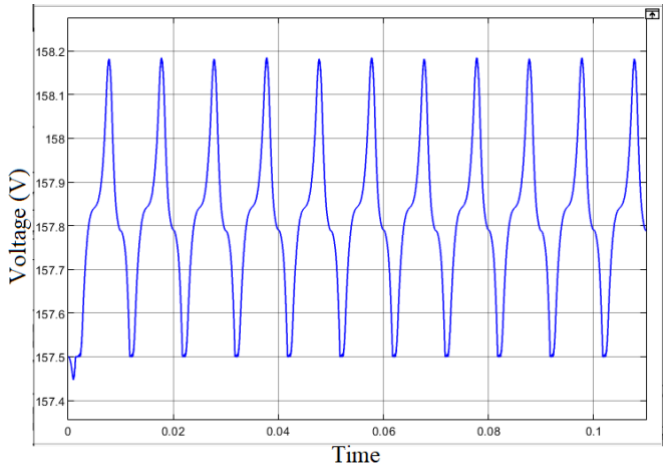


Fig. 11. The ripple of the DC-link voltage

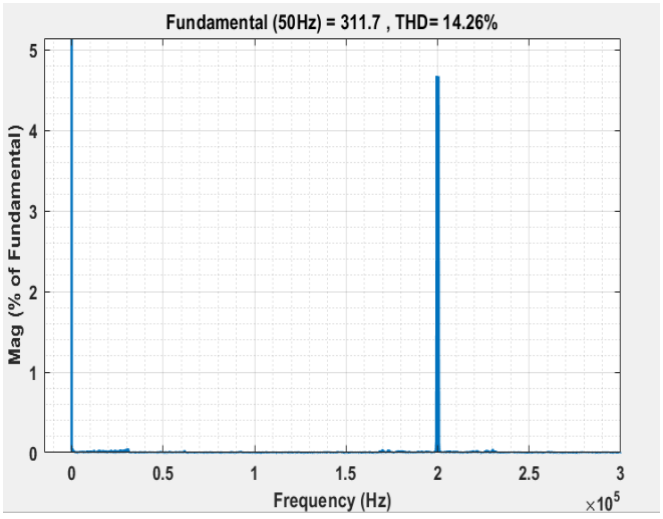
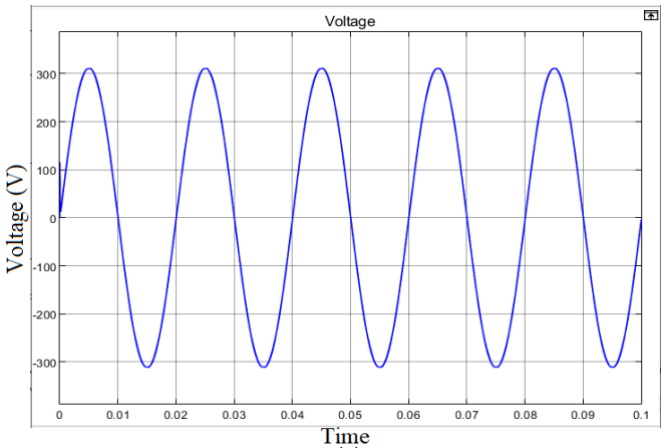
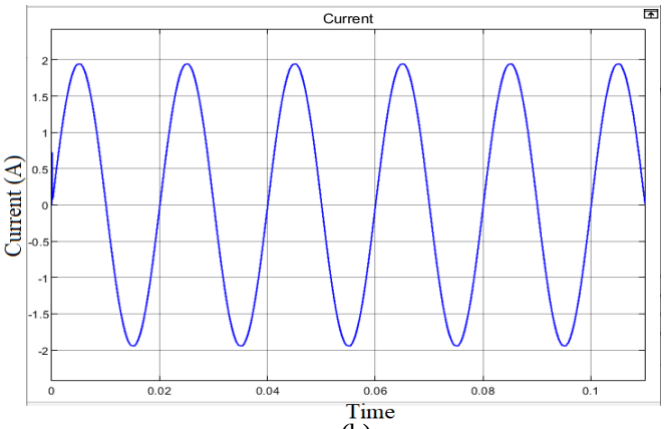


Fig. 12. FFT analysis for PS-PWM method

Fig. 13 display the effect of adding L-filter for PEC-9 with PS-PWM mechanism. The THD of the output waveform is reduced as presented in Fig.14 and equal to 0.34%. Has been assumed 0.99 modulation index for both modulation methods. In comparison with level-shift approach at the same switching frequency and with the same parameters, the results indicated that the THD of the output signal is much reduced when the PS-PWM method is implemented.



(a)



(b)

Fig. 13. Output waveforms for PS-PWM method with filter; a) voltage; b) current

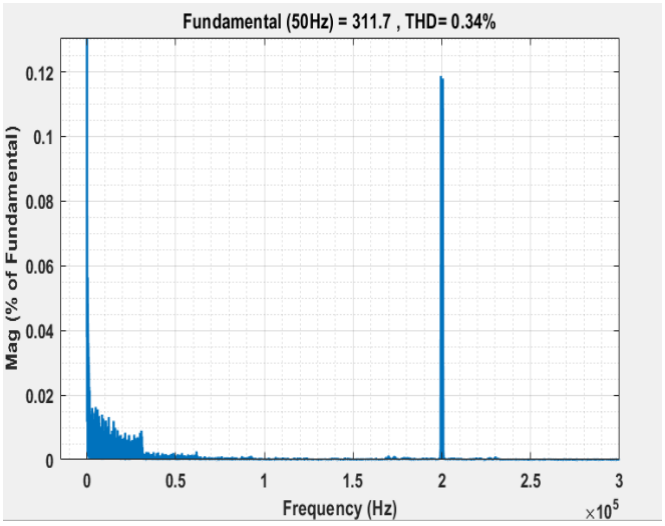


Fig. 14. FFT analysis for PS-PWM method with filter

5. Conclusion

To reduce the THD of the nine-level PEC inverter, PS-PWM scheme has been performed in this paper. The results shows that when using PS-PWM technique, the harmonic orders shifted to the higher away from the fundamental frequency as the multiple order of the switching frequency. Therefore, the THD decreased significantly. The dominant harmonics of the output signal are around eight-times of the switching frequency and hence, this lead to minimize the output filter size. The PS-PWM method is better for enhance the power′s quality and improve the inverter performance than the PDLS-PWM.

References

[1] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. Prats, "The age of multilevel converters arrives," Industrial Electronics Magazine, IEEE, vol. 2, pp. 28-39, 2008.

[2] P. Qashqai, A. Sheikholeslami, H. Vahedi, and K. Al-Haddad, “A Review on Multilevel Converter Topologies for Electric Transportation Applications,” in Proc. VPPC, pp. 1 – 6, 2015.

[3] C. Buccella, M. G. Cimoroni, C. Cecati, L. A. Disim, and L. Aquila, “Low-frequency harmonic elimination technique in three phase cascaded H-bridges multilevel inverters for renewable energy applications,” International Journal of Smart Grid - ijSmartGrid, vol. 3, no. 1, p. 9 Pages, 2019.

[4] M. Saeedian, J. Adabi, and S. M. Hosseini, "Cascaded multilevel inverter based on symmetric–asymmetric DC sources with reduced number of components," IET Power Electronics, vol. 10, no. 12, pp. 1468-1478, 2017.

[5] E. Samadaei, A. Sheikholeslami, S.-A. Gholamian, and J. Adabi, ‘‘A square T-type (ST-Type) module for asymmetrical multilevel inverters,’’ IEEE Trans. Power Electron., vol. 33, no. 2, pp. 987–996, Feb. 2018.

[6] E. Samadaei, S. A. Gholamian, A. Sheikholeslami, and J. Adabi, ‘‘An envelope type (E-type) module: Asymmetric multilevel inverters with reduced components,’’ IEEE Trans. Ind. Electron., vol. 63, no. 11, pp. 7148–7156, Nov. 2016.

[7] adaei, M. Kaviani, and K. Bertilsson, ‘‘A 13-levels module (K-Type) with two DC sources for multilevel inverters,’’ IEEE Trans. Ind. Electron., vol. 66, no. 7, pp. 5186–5196, Jul. 2019.

[8] H. Samsami, A. Taheri, and R. Samanbakhsh, ‘‘New bidirectional multilevel inverter topology with staircase cascading for symmetric and asymmetric structures,’’ IET Power Electron., vol. 10, no. 11, pp. 1315–1323, Sep. 2017.

[9] S. S. Lee, M. Sidorov, C. S. Lim, N. R. N. Idris, and Y. E. Heng, ‘‘Hybrid cascaded multilevel inverter (HCMLI) with improved symmetrical 4-level submodule,’’ IEEE Trans. Power Electron., vol. 33, no. 2, pp. 932–935, Feb. 2018.

[10] Mokhberdoran and A. Ajami, ‘‘Symmetric and asymmetric design and implementation of new cascaded multilevel inverter topology,’’ IEEE Trans. Power. Electron., vol. 29, no. 12, pp. 6712–6724, Dec. 2014.

[11] Taghvaie, J. Adabi, and M. Rezanejad, ‘‘A self-balanced step-up multilevel inverter based on switched-capacitor structure,’’ IEEE Trans. Power Electron., vol. 33, no. 1, pp. 199–209, Jan. 2018.

[12] Taghvaie, J. Adabi, and M. Rezanejad, ‘‘A multilevel inverter structure based on a combination of switched-capacitors and DC sources,’’ IEEE Trans. Ind. Informat., vol. 13, no. 5, pp. 2162–2171, Oct. 2017.

[13] X. Xiang, X. Zhang, T. Luth, M. M. C. Merlin, and T. C. Green, ‘‘A compact modular multilevel DC–DC converter for high step-ratio MV and HV use,’’ IEEE Trans. Ind. Electron., vol. 65, no. 9, pp. 7060–7071, Sep. 2018.

[14] K. Al-Haddad, Y. Ounejjar, and L. A. Gregoire, "Multilevel Electric Power Converter," US Patent 20110280052, 2011.

[15] H. Vahedi, K. Al-Haddad, and H. Y. Kanaan, "A New Voltage Balancing Controller Applied on 7-Level PUC Inverter," in IECON 2014-40th Annual Conference on IEEE Industrial Electronics Society, USA, 2014, pp. 5082-5087: IEEE.

[16] H. Vahedi and K. Al-Haddad, "PUC5 Inverter–A Promising Topology for Single-Phase and Three-Phase Applications," in IECON 2016-42nd Annual Conference of the IEEE Industrial Electronics Society, Italy, 2016.

[17] M. Sharifzadeh and K. Al-Haddad, "Packed E-Cell (PEC) Converter Topology Operation and Experimental Validation," IEEE Access, vol. 7, pp. 93049-93061, 2019.

[18] S. Arazm, H. Vahedi, and K. Al-Haddad, "Generalized Phase-Shift Pulse Width Modulation for Multi-Level Converters," in 2018 IEEE Electrical Power and Energy Conference (EPEC), 2018, pp. 1-6: IEEE.

[19] M. Babaie, M. Sharifzadeh, M. Mehrasa, G. Chouinard and K. Al-Haddad, "PV Panels Maximum Power Point Tracking based on ANN in Three-Phase Packed E-Cell Inverter," 2020 IEEE International Conference on Industrial Technology (ICIT), pp. 854-859, 2020.

[20] S. Arazm, H. Vahedi, and K. Al-Haddad, "Phase-shift modulation technique for 5-level packed U-cell (PUC5) inverter," in 2018 IEEE 12th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG 2018), pp. 1-6, 2018.

[21] Muhammad H. Rashid, POWER ELECTRONICS HANDBOOK: Butterworth-heinemann, 2017.

[22] M. Ahmadijokani, M. Sharifzadeh, M. Mehrasa, F. Sebaaly and K. Al-Haddad, "Modified Level-Shifted PWM Technique With Active DC Capacitors Voltages Balancing for Nine-level Packed E-Cell (PEC9) Inverter," IEEE International Conference on Industrial Technology (ICIT), pp. 843-848, 2020.

[23] E. S. Mohammed and K. S. R. Rao, “A New Multi Carrier Based PWM for Multilevel Converter,” Applied Power Electronics Colloquium, pp. 63-68, May 2011.